A High Performance Sigma-Delta ADC for Audio Decoder Chip

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Abstract
This paper gives a high performance sigma delta Analog to Digital Converter (ADC) applied in computer audio decoder chip. In this design, a 3rd-order single-loop CIFF topology is chosen to achieve the high performance ADC. Its signal bandwidth is 20 KHz, sampling frequency is 10.24MHz and oversampling ratio is 256. Local feedback coefficient \( g \) is used to reduce quantization noise. The non-linear model of modulator is given and the stability is analyzed. It is got that when quantizer gain is bigger than 0.322 the system is stable. According to simulation, Signal to Noise Ratio (SNR) is 123.1dB and Effective Number of Bits (ENOB) is 20.15bits. When input level is bigger than -3dBFS, the modulator is overload and becomes unstable. Then the integrator, quantizer and feed forward summation in ADC circuit are designed. Then the ADC is implemented in 0.6um CMOS process, and the test result shows that its performance is 99.28dB.

Keywords: Sigma Delta, Loop Stability, Audio Decoder

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requires a very good manufacturing process. And MASH modulator has digital part, which would increase the complexity of the circuit. In this design, single loop structure is chose [14-15].

Figure 1. Block Diagram of 3rd-order \( \Sigma\Delta \) ADC System

Single loop modulator has two main structures: Chain of Integrators with weighted FeedForward summation (CIFF structure) and Cascade of Integrators with distributed Feedback (CIFB structure). CIFF structure is a wonderful structure to realize Butterworth filter and its signal transfer function is flat in signal bandwidth. In CIFB structure the input and output of integrators include signal and quantizer output, so the amplitude of integrators’ input and output is very big. Little gains are required in CIFB structure. The gain in switch-capacitor circuit is realized by proportional capacitors. Little gains means big capacitors which would lead to more power consumption and bad output settle. CIFF structure has more advantages than CIFB structure [15-17]. So this paper also chooses the CIFF structure.

For sigma-delta ADC, the higher order and higher oversampling ratio achieve higher precision. In computer audio application, 16 bit precision is needed. So in this paper a third-order single loop CIFF structure modulator is designed. The signal bandwidth is 20KHz, oversampling ratio is 256, and the sampling clock is 10.24MHz. The third-order sigma-delta ADC topology is shown as Figure 1. There are three integrators, a one bit quantizer and gains.

In this modulator, the open loop transfer function \( L_0(z) \) can be written as follow:

\[
L_0(z) = \frac{a_1b_1}{(z-1)} - \frac{a_2b_2b_1(z-1) + a_3b_3b_2b_1}{(z-1)((z-1)^2 + b_1b_2g_1)}
\]  
(1)

Where \( a_1, a_2, a_3, b_1, b_2 \) and \( b_3 \) are the proportional capacitances in circuit. The feedback transfer function \( L_1(z) \) can be written as:

\[
L_1(z) = 1 + \frac{a_1b_1}{(z-1)} + \frac{a_2b_2b_1(z-1) + a_3b_3b_2b_1}{(z-1)((z-1)^2 + b_1b_2g_1)}
\]  
(2)

From the open loop transfer function \( L_0(z) \) and the feedback transfer function \( L_1(z) \), the signal transfer function (STF) and quantizer noise transfer function (NTF) can be written as follows:

\[
STF(z) = \frac{L_1(z)}{1 - L_0(z)} = 1
\]  
(3)

\[
NTF(z) = \frac{1}{1 - L_0(z)} = \frac{1}{1 - \frac{a_1b_1}{(z-1)} - \frac{a_2b_2b_1(z-1) + a_3b_3b_2b_1}{(z-1)((z-1)^2 + b_1b_2g_1)}}
\]  
(4)
The STF is always equal to one which ensures no loss of signal. The NTF shows a high-pass filter characteristic to reduce quantization noise in bandwidth.

![Figure 2. Zeros and Poles of Third-order Butterworth Filter](image1)

![Figure 3. NTF Transfer Characteristic with \( g_1 \) and without \( g_1 \)](image2)

The next step for system design is to choose a high-pass filter transfer function for noise transfer function. The most commonly used filter transfer function is Butterworth filter, Chebyshev I filter and Chebyshev II filter. The Butterworth filter function has advantages like passband flatness, inhibition of excessive band gain and good stability. Therefore the Butterworth filter function is picked as the noise transfer function. Butterworth transfer function is shown as follow:

\[
H(z) = \frac{(z-1)^r}{D(z)}
\]  

(5)

The poles and zeros of third-order Butterworth filter are shown as Figure 2. The zeros are all set around the real value one to suppress quantization noise in baseband. The poles are all set appropriately in unit circle to make the system stable. The Butterworth filter’s poles and zeros correspond to poles and zeros of NTF. So the gain coefficients like \( a_1, a_2, a_3, b_1, b_2 \) and \( b_3 \) can be got from the zeros and poles as Table 1. To increase noise-shaping ability in signal baseband, the local feedback coefficient \( g_1 \) is added into last two integrators in modulator system. The local feedback \( g_1 \) split two zeros not slightly off real value one. This generates a minimum value for noise transfer function in signal baseband. The NTF transfer characteristic with \( g_1 \) and without \( g_1 \) are plotted in Figure 3. From the Figure 3, it is got that NTF with \( g_1 \) has better noise-shaping ability than NTF without \( g_1 \).

<table>
<thead>
<tr>
<th>Gain</th>
<th>( a_1 )</th>
<th>( a_2 )</th>
<th>( a_3 )</th>
<th>( b_1 )</th>
<th>( b_2 )</th>
<th>( b_3 )</th>
<th>( g_1 )</th>
</tr>
</thead>
<tbody>
<tr>
<td>Value</td>
<td>1.877</td>
<td>2.183</td>
<td>2.46</td>
<td>0.427</td>
<td>0.31</td>
<td>0.135</td>
<td>0.002</td>
</tr>
</tbody>
</table>

### 3. Stability Analysis

In traditional computer audio sigma-delta ADC system, it is always considered as a linear system. The quantizer in modulator has gain as big as one. However the modulator system is not a linear system. The quantizer has a gain \( k_q \).

The nonlinear model of the third-order sigma-delta modulator system is described as Figure 4. In figure quantizer consists of gain \( k_q \) and quantization noise. The quantizer gain \( k_q \) is a variable changed with ADC input. So the whole modulator system is conditionally stable.
There is a range of $k_q$ that make sure the system is stable. The nonlinear noise transfer function is:

$$NTF(z) = \frac{1}{1 - k_q L_0(z)} = \frac{(z - 1)[(z - 1)^2 + b_0 g_1]}{[(z - 1) + k_q a_1](z - 1)^2 + b_0 g_1] + k_q a_1 b_2 (z - 1) + k_q a_1 b_2 b_3}$$  \hspace{1cm} (6)$$

Limit cycle is used to calculate the range of $k_q$. Based on Equation (6), the limit cycle of third-order signal-delta modulator is plotted in Figure 5. From the limit cycle result, it got that when the quantizer gain is bigger than 0.322 the system is stable.


The designed third-order sigma-delta modulator system is simulated by Simulink. In simulation the input signal is 100KHz sine wave, sampling frequency is 10.24MHz and signal bandwidth is 200KHz. The output Power Spectrum Density (PSD) is shown as Figure 6. The SNR is 123.1dB and ENOB is 20.15 bits. The performance satisfies the demand of computer ADC decoder.

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Figure 4. The Nonlinear Model of Sigma-delta System

Figure 5. Limit Cycle of Third-order Modulator System

Figure 6. PSD of Modulator Output

Figure 7. Relation between SNR and Input Level
The relation between SNR and input level is described in Figure 7. When input level is smaller than -3dBFs, SNR is almost linear with input level. When input level is bigger than -3dBFs, the modulator is overload and becomes unstable.

5. Circuit Module in ADC
5.1. Integrator in ADC

The integrator used in this ADC is the same phase switch-capacitor integrator. Its work principle is: when \( P1 \) is high, the switch \( S1, S3 \) are turned on, \( P2 \) is low and the switch \( S2, S4 \) are turned off. In this time the input signal of integrator charges the sample capacitor \( C1 \). When \( P1 \) is low, the switch \( S1, S3 \) are turned off, \( P2 \) is high and the switch \( S2, S4 \) are turned on. In this time electric in \( C1 \) is transmitted into integrate capacitor \( C2 \).

According to conservation of charge, the amount of electric in sample capacitor \( C1 \) is equal to the amount of electric change in integrating capacitor \( C2 \). The equation can be written as follow:

\[
[V_{out}(nT + T) - V_{out}(nT)]C2 = V_{in}(nT)C1
\]

(7)

Write the equation into Z-transform, it gets the transform function of switch-capacitor integrator:

\[
I(z) = \frac{V_{out}(z)}{V_{in}(z)} = \frac{C1}{C2} \frac{z^{-1}}{1 - z^{-1}} = \frac{C1}{C2} \frac{1}{z - 1}
\]

(8)

The capacitor ratio \( C1/C2 \) is used to realize the integrator gain \( b_1, b_2 \) and \( b_3 \). In this integrator clock \( P1 \) and \( P2 \) have delay clock \( P1d \) and \( P2d \) to turn off \( S1 \) and \( S2 \) advance. This can prevent interference of switch charge injection to sample capacitor \( C1 \).

The amplifier used in this integrator is plotted in Figure 9. It is a folded cascode two-stage miller amplifier. \( M1 \) and \( M2 \) is the input mosfet and use the PMOS to decrease the 1/f noise. \( M13 \) and \( M11 \) constitute current mirror to supply the bias voltage for \( M12, M5, M6, M9 \) and \( M10 \). Current mosfet to supply current for first stage. \( M1, M4, M7, M8 \) are cascode mosfet to increase gain of amplifier. Gate voltage of \( M5 \) and \( M6 \) are provided by source port of \( M3 \) to increase the output swing of first stage. Miller capacitor \( C1 \) is used to compensate the first pole and second pole in amplifier to insure stability of amplifier. The second stage is made up by \( M13 \) and \( M14 \). Though the second stage gain is low, it improves the amplifier output swing. \( C1 \) is the load capacitor in output.

The gain of this amplifier is :
\[ A_v = g_{m3} (g_{m5} r_{e5}) \parallel (g_{m7} r_{e7}) g_{m13} (r_{e13} \parallel r_{e14}) \]  

(9)

Where \( g_{m1} \), \( g_{m3} \), \( g_{m7} \) and \( g_{m13} \) are the transconductance of \( M_1 \), \( M_3 \), \( M_7 \) and \( M_{13} \). \( r_{e5} \), \( r_{e7} \), \( r_{e13} \) and \( r_{e14} \) are resistors between source and drain of \( M_5 \), \( M_7 \), \( M_{13} \) and \( M_{14} \).

Implemented in 0.6um CMOS process, the gain of amplifier is 81.2dB, unit gain bandwidth is 41.3MHz. When load capacitor is 10pF, the phase margin is 62.3°. The rising slew rate is 40.2V/us and the falling slew rate is -38.6V/us. The input swing is 0.1-3.8V and output swing is 0.1-4.7V.

5.2. Quantizer in ADC

The quantizer in this ADC is realized by a one-bit comparator. When input signal is higher than middle voltage, the output would be a high signal. When input signal is lower than middle voltage, the output would be a low signal. In ADC it requires quantizer to distinguish as low as minimum voltage, behave fast and ability to latch the result.

![Figure 10. One-bit Quantizer Circuit](image)

The circuit of quantizer is shown in Figure 10. It is a dynamic comparator with latch. When the clock control signal is low, the nodes \( P \) and \( Q \) are preset with supply voltage. When the clock control signal is high, presetted nodes \( P \) and \( Q \) discharge respectively through \( M_{2a} \) and \( M_{2b} \). When the node voltage of the \( P \) and \( Q \) is lower than the threshold voltage of the MOS transistor, the latter two inverters of the latch to change the value of the original the \( outn \) and \( outp \), until it reaches the voltage value comparison. The result is latched in quantizer. The power consumption of the quantizer is very low and its comparison speed is very fast.

With the advancement in networking and multimedia technologies enables the distribution and sharing of multimedia content widely. In the meantime, piracy becomes increasingly rampant as the customers can easily duplicate and redistribute the received content. Although encryption can provide multimedia content once a piece of digital content is decrypted, the dishonest customer can redistribute it arbitrarily.

6. Test and Discussion

The ADC is fabricated in 0.6um CMOS process. The power spectrum density of the ADC is obtained by the oscilloscope in Figure 11. The test result shows that the SNR of this ADC is 99.28dB and ENOB is 16.2bits. The test result is lower than simulation, because the electronic noise in circuit affects the performance of ADC. The single-end amplifier applied in this ADC result in non-linearity and this brings up the harmonic in signal bandwidth. So to increase the performance of ADC, it is advised to use correlated double sample to decrease electronic noise and employ fully differential circuit to increase linearity to suppress harmonic.
7. Conclusion

This paper presents design of high performance sigma-delta ADC applied in audio decoder chip. The CIFF third-order sigma-delta modulator system is analyzed. The Butterworth filter function is used to realize the NTF of modulator. Based on nonlinear model, it is got that when the quantizer is bigger than 0.322 the system is stable. Through Simulink simulation, the SNR of system is 123.1dB and ENOB is 20.15bits. The performance satisfies the demand of computer ADC decoder. From the output histograms of three integrators, it is gotten that the output ranges of three integrators satisfy the limit of integrators. And SNR is almost linear with input level. When input level is bigger than -3dBFs, the modulator is overload. The test result shows that the SNR of this ADC is 99.28dB and ENOB is 16.2bits. The single-end amplifier in this ADC brings up the harmonic in signal bandwidth.

References