Effects of Non-Uniform Channel Geometry on Double-Gate MOSFET Performance

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Abstract
A Double-gate (DG) MOSFET with non-uniform channel (NUC) geometry, that is, the silicon thickness of embedded in double-gate is varied linearly from drain to source, is proposed. To quantitatively assess the effects of the NUC geometry on electrical characteristics of DG MOSFETs, the short-channel effects (SCEs) and the on-state current are numerically calculated for the device with different non-uniform channel thickness, channel length and gate oxide thickness respectively. To the proposed structure, the SCEs are suppressed, the subthreshold swing becomes smaller and the on-state current is significantly improved when the thickness of silicon lied at source becomes thinner, showing better performances than the conventional DG MOSFETs.

Keywords: double gate MOSFETs, non-uniform channel geometry, short-channel effects, on-state current

1. Introduction
Compared with conventional single-gate MOSFETs, Double-gate (DG) MOSFETs have obvious advantages, such as suppression of short channel effects (SCEs), lower subthreshold swing (SS) and higher transconductance, so they have attracted a great deal of attention in recent years [1-8]. In theory, DG MOSFETs can be scaled to the shortest channel length possible for a given gate oxide thickness [9]. However, when the channel length is aggressively scaled down, the two dimensional electrostatic effects become relevant, and the electrostatic controllability of the gate over the channel decreases due to the increased charge sharing from source/drain [10], so the performances of scaled down DG MOSFETs are limited.

Among the previous reports, the effects of silicon thickness ($t_{si}$) [1-5], channel length ($L$) [1-3], gate oxide thickness ($T_{ox}$) [3,6], source/drain doping concentration ($N_{SD}$) [6] and channel doping concentration ($N_{CH}$) [6,7] on the performances of the DG MOSFETs have been investigated. It is found that the device with a shorter channel length does slightly enhance the on-state current, but SS becomes large simultaneously. The device with thinner silicon thickness can enhance the controllability of gate electrodes, greatly suppresses the SCEs, but when the silicon thickness is reduced to about 10nm, owing to the mobility degradation and the reduction of the electron charge density, the on-state current issue suffers [2], [4-5].

To address the issues of the conventional DG MOSFETs mentioned above, obtain an optimized device performance, a tradeoff between channel length and silicon thickness should be appropriate, which is known that $L / t_{si} \geq 1$ has been reported [2]. While the analysis in Ref. [2] was focused on the conventional DG MOSFETs with uniform channel thickness, the effect of silicon geometry on the performance of DG MOSFET has not been studied in detail. Based on this point, a DG MOSFET with non-uniform channel (NUC) geometry is proposed.

In this paper, a systematic study on NUC DG MOSFETs with variable silicon thickness at source edge is performed. The performances of the NUC DG MOSFETs are evaluated by considering the electrical characteristics: 1) the short-channel effects ($V_{t}$, SS); 2) the on-state current. The proposed device in this paper combines the advantages of shorter channel length and thinner silicon thickness to enhance the on-state current. In addition, the SCEs are suppressed and the subthreshold swing becomes smaller.
2. Device Structure and Simulation Model

Figure 1 shows the schematic diagram of the simulated NUC DG MOSFET structure. Here, the NUC geometry is represented by linear variation of silicon thickness from the drain to the source. While the thickness of silicon lied at drain edge is fixed to 40nm, the thickness of silicon lied at source edge ($T_{si}$) is varied. The effects of the different channel length and gate oxide thickness on the characteristics of NUC DG MOSFETs will be simulated as well. The gate material is $n^+$ polysilicon with fixed doping concentration of $10^{20}$ cm$^{-3}$, the channel region is doped with boron concentration ($N_{CH}$) of $10^{15}$ cm$^{-3}$, the source and the drain regions are doped with phosphorous concentration ($N_{SD}$) of $10^{20}$ cm$^{-3}$. The simulation is performed using Silvaco [11].

3. Results and Discussion

3.1. Suppression of Short-channel Effects

Figure 2 shows the comparison of $V_T$ and $SS$ of the NUC DG MOSFETs with different $T_{si}$. For the lightly doped NUC DG MOSFETs, as $T_{si}$ increases, the monotonic decreasing of $V_T$ is ascribed to the special volume inversion effect. In the strong-inversion region, the special volume inversion effect will become insignificant that was not predicted by the linearly extrapolated $V_T$ in [6, 8]. Moreover, for thinner channel thickness, the series resistance of the source/drain extension region overlapped by the gate may become larger, so the $V_T$ increases [3].

Figure 2. $T_{si}$ Dependence of $V_T$ and SS for NUC DG MOSFETs

Compared to the conventional DG MOSFETs with uniform channel thickness (i.e., $T_{si}$= $t_{si}$=40nm), the $SS$ of NUC DG MOSFETs becomes smaller with $T_{si}$ decreasing, as shown in Figure 2(b). For DG MOSFETs with nanoscale channel thickness, the dopant in channel will
introduce an additional electric field called channel dopant-induced field \( U_{1D}(y) \) \([1]\), this electric field can be expressed as follows:

\[
U_{1D}(y) = \frac{V_a}{2} \left( \frac{y^2}{t_w^2} - \frac{1}{4} \right)
\]

(1)

Where all the notations can be found in \([1]\). The decreased \( t_w \) would enhance the channel dopant-induced field, which will greatly enhance the surface potential \( (y = \pm t_w / 2) \). Since the surface potential becomes much larger than the central potential \( (y = 0) \), the overall conduction path will be highly confined to the channel surfaces, causing an enhanced gate control and a smaller \( SS \) \([1]\).

For NUC DG MOSFETs, with decreasing \( T_{si} \) values, an enhanced dopant-induced field \( U_{1D}(y) \) will also enhance the surface potential near source \( (y = \pm T_{si} / 2) \). Once it is much larger than the central potential \( (y = 0) \), resulting in an improved \( SS \). In other words, the \( SS \) of NUC DG MOSFETs is sensitive to the thickness of channel near source, so the dimensions of NUC DG MOSFETs are scaled down more easily, results in improving integration.

Figure 3. \( L \) Dependence of \( V_T \) and \( SS \) for NUC DG MOSFETs

Figure 3 compares the \( L \) dependence of \( V_T \) and \( SS \) for NUC DG MOSFETs and conventional DG MOSFETs, measured at \( V_{ds} = 0.05V \). It is found that \( V_T \) decreases significantly with decreasing \( L \) for all devices, which is caused by SCEs and can be explained by charge sharing model \([10]\). NUC DG MOSFETs with a thinner \( T_{si} \) sustain a good \( V_T \) rolloff behavior than that of the conventional DG MOSFETs due to the fact that the charge sharing effect is substantially reduced with decreasing \( T_{si} \) \([5]\). It is also worth noticing that the sensitivity of the \( SS \) with the channel length is lower in NUC DG MOSFETs than in conventional DG MOSFETs, because the NUC DG MOSFET with thinner \( T_{si} \) is well controlled by the gate, leading to improved electrical properties \([1, 5]\).

Figure 4 shows the \( TOX \) dependence of \( V_T \) and \( SS \) for NUC DG MOSFETs. According to the slope of the plots illustrated in Figure 4(a) and (b), it is found that the parameters of \( V_T \) and \( SS \) are influenced weakly by \( TOX \), making this an important useful feature of the NUC DG MOSFETs. Hence, it indicates that the \( TOX \) can be further scaled down for a given channel length and other device parameters. Based on the above discussions, it can be concluded that the novel structure can suppress the SCEs of DG MOSFETs effectively, which may provide a good alternative in scaling down of devices.
3.2. Improvement of On-state Current

Figure 5 shows the drain current of NUC DG MOSFETs and conventional DG MOSFETs. It can be clearly seen that the NUC DG MOSFETs exhibit significant performance enhancement. For conventional DG MOSFETs, according to channel dopant-induced field effect [1], the reduction of the silicon thickness effectively cuts off the bulk charge and inversion charge, which results in a considerable change of the electron concentration distribution to get the same effective electric field. This results in an increase of the drain current due to a small increase of the effective mobility [4]. But when the thickness of silicon is ultrathin, the effective mobility will be degraded due to enhanced phonon and severe surface-roughness scattering, meanwhile, the inversion layer charge density will be decreased due to the channel overlap effect. Consequently, the drain current of the conventional DG MOSFET with ultrathin silicon thickness decreases drastically.

However, changing the geometry of channel will cause two effects: 1) An increase of the effective mobility due to the increase of the average electron distance from the surface, 2) An increase of the electron density due to the reduced influence of the channel overlap effect. These effects will result in a significant increase of the drain current for NUC DG MOSFETs, as shown in Figure 5. It is shown that the on-state current is considerably enhanced in case of NUC DG MOSFETs even for the thickness of silicon lied at source edge $T_s$ down to 5nm. That means the NUC DG MOSFETs can be scaled to the thinnest silicon thickness at source edge $T_s$ possible for a given channel length and other device parameters.
4. Conclusion

In this paper, based on the simulation, the effects of NUC geometry on the performances of DG MOSFETs are symmetrically studied by varying $L$ and $T_{Ox}$ on NUC DG MOSFETs with different $T_{si}$. It is found that NUC DG MOSFETs with thinner silicon thickness at source edge $T_{si}$ can not only suppress the SCEs, but also greatly enhance the on-state current. Additionally, the parameters of $V_T$ and $SS$ are influenced weakly by the channel length and the gate oxide thickness, these good characteristics show that NUC DG MOSFETs are more immune to short channel effects, which is another advantage since the downscaling of device dimensions can result in improving the IC performance.

Acknowledgements

This work was supported by the National Youth Science Foundation of China (Grant No. 61006064), Anhui provincial natural science research project (Grant No. KJ2011B008) and the Natural Science Foundation of Education Office Anhui Province (No. KJ2013A071).

References