Compensator Based Performance Enhancement Strategy for a SIQO Buck Converter

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1. INTRODUCTION

The present day consumer electronics require multiple levels of supply voltages for their core modules. Besides in light of the view that the low drop out regulators reduce the conversion efficiencies at heavy load, they are replaced by the switch mode converters which provide the desired voltage levels in both magnitude and polarity. However the inductors present in each converter occupy large space and increase the cost of the whole system. Single Inductor Multiple Output (SIMO) converters offer advantages of using a single inductor which usually occupies less space for any number of outputs. However there is a need for an efficient controller which actually time shares the inductor current among all the outputs at different voltage/current levels such that the desired time domain specifications are obtained with reduced cross regulation and ripple.

A substantial work on SIMO converters are seen in the literature in the field of designing controllers. In [1], for a SIMO converter, load independent control through the sum of each output’s phase difference and the freewheeling current have been used to generate the control signal such that the output of the converter has less under shoot or over shoot at load transients. The efficiency has been seen to be maximum at steady state since the freewheeling current duration is zero. Converters with single inductor capable of providing Buck and Boost configuration with independent control of each output is used to minimize the cross regulation between the outputs and obtain the desired regulatory characteristics using separate regulation of common mode and differential mode voltages by developing the non-linear functional gain blocks [2]. The converter has been able to regulate both buck and boost outputs by controlling the conducting period of the devices. In [3], the current accumulation problem was reduced along with high...
conversion efficiency by delivering the input energy to the outputs through a lossless inductor continually. The steady state and the dynamic responses with nominal load change have been improved by designing the non-linear controller considering the saturation of control signals and the switching losses [4]. A hybrid topology has been developed by combining the class AB amplifier with the switching converter in order to enhance the transient response and minimize the cross regulation. The class AB amplifier has been seen to act faster than the switching converter and feed load transient current to suppress the effects of cross regulation [5]. A single shared hysteresis comparator has been used to regulate the output voltages and the time limited power distribution control used to suppress the cross regulation [6]. A power multiplexed discontinuous conduction mode switching scheme has been proposed for SIMO output dc-dc power converter to nullify the cross regulation and improve the dynamic and steady state performances of the system [7]. The analog implementation of PWM based sliding mode controller [8] along with internal integral control loop has been implemented for suppressing the cross regulation and steady state regulation error in a single inductor dual output dc-dc buck converter. In [9], ripple based adaptive off time control circuit is designed which does not require error amplifier or PWM compensation. The operating frequency is locked to the reference clock. The controllers discussed above use complicated algorithms and are not obtained from a mathematical procedure and complex circuits are used to implement the developed algorithms.

Modeling of dc-dc converters plays vital role to analyze the performance of the converter. The developed model will help to determine the parameters of the conventional or linear or non-linear controllers using optimization techniques. AC modeling and small signal transfer function of a single input single output dc-dc converter [10] are developed by considering the non-ideal components of Buck converter. For the same buck converter [11], novel small signal averaged model is developed when it operates at variable switching frequency. A generalized state space averaging technique has been used to obtain the dynamic model of buck converter along with sliding mode controller. The use of artificial intelligent techniques has been used to obtain the optimum values of the controller and enable the reduction in computational simulation time [12].

For a dual output, a digital implementation of multivariable gain controller is developed using a model developed in steady state in such a way that the diagonal elements are used to improve the regulatory performance of the converter and the off diagonal elements are used to suppress the cross regulations [13]. However the algorithm used to develop a model is complex and restricted to two outputs. A ripple based modeling of single inductor dual output buck converter is also developed for a cross derivative state feedback control methodology [14]. In another research, an inductor current ripple-based modeling approach has been proposed to accurately model and analyze the converter. The control, cross-coupling, and cross-regulation transfer functions, generated through the model has been portrayed [15]. But the procedure used is very complex and lengthy.

In this paper the mathematical modeling of the Single Inductor Quad Output (SIQO) converter is developed by state space averaging technique which can be extended for any number of outputs easily. Further transfer function model is developed from lumped small signal equivalent circuit. Additionally, SIMO converters operated on open loop do not give satisfactory results at transients as well as under steady state conditions. Therefore compensators are designed and incorporated in each output using frequency and time domain specifications. The converter is developed in MATLAB/SIMULINK® using discrete components and its performance is analyzed with and without compensators and it is established that the excellent results are obtained using lag and lag-lead compensators. The performance of the converter so designed is validated using DT 9834® DAQ module.

2. SYSTEM DIAGRAM AND OPERATION

Figure 1 shows the circuit diagram of single input four output dc-dc buck converter with single inductor. The converter can be operated in the continuous conduction mode (CCM), discontinuous conduction mode (DCM) and pseudo continuous conduction mode (PCCM) of operation. The mode of operation is decided based on the amount of ripples allowed, the load current rating and the converter efficiency. The continuous mode of operation enables to handle large amount of current with less amount of ripples and produce the high conversion efficiency but suffers from the effects of cross regulation. The effort in this investigation revolves to arrive at compensators for enhancing its performance in this perspective. The switching scheme of the converter for one switching cycle operating in continuous conduction mode of operation is shown in Figure 2. \( S_p \) and \( S_p' \) form the main path and \( S_1, S_2, S_3 \) and \( S_4 \) form sharing paths. Figure 2(a) shows the switching pulses for the switches in sharing path and Figure 2(b) shows the switching pulses for the switches in main path for the SIQO converter. Figure 3 shows the timing diagram of inductor current for one switching cycle.

Compensator Based Performance Enhancement Strategy for a SIQO Buck Converter (S. Augusti Lindiya)
The state space model of the converter for each mode of operation is obtained by using Kirchhoff’s voltage and current laws by considering the four output voltages ($v_1, v_2, v_3$ and $v_4$) and the inductor current ($i_L$) as state variables. The duty cycles $d_1, d_2, d_3$ and $d_4$ are the independent control variables. The disturbances are observed at the input voltage ($v_{in}$) and the load currents ($i_1, i_2, i_3$ and $i_4$) and $R_{on}$ is the on state resistance of the conducting switches to represent the conducting losses.

![Circuit diagram of SIQO dc-dc converter](image1)

Figure 1. Circuit diagram of SIQO dc-dc converter

![Switching pulses of the SIQO converter](image2)

Figure 2. Switching pulses of the SIQO converter
2.1. Mode 1 Operation

In this mode, the capacitor in output 1 gets charged from the input supply by turning on the switches $S_1$ and $S_p$ and the differential equations obtaining for voltage across the inductor and current passing through the capacitor are written in state space form as in Equations (1) and (2).

\[
\begin{bmatrix}
\frac{1}{C_1} & 0 & 0 & 0 \\
0 & \frac{1}{R_1C_1} & -\frac{1}{L} & 0 \\
0 & 0 & -\frac{1}{R_2C_2} & 0 \\
0 & 0 & 0 & -\frac{1}{R_3C_3}
\end{bmatrix}
\begin{bmatrix}
\dot{i}_L \\
\dot{v}_1 \\
\dot{v}_3 \\
\dot{v}_4
\end{bmatrix}
= \begin{bmatrix}
-R_{on}
\end{bmatrix}
\begin{bmatrix}
i_L \\
v_1 \\
v_3 \\
v_4
\end{bmatrix}
\]

\[
\begin{bmatrix}
1 \\
0 \\
0 \\
0
\end{bmatrix}
\begin{bmatrix}
i_L \\
v_1 \\
v_3 \\
v_4
\end{bmatrix}
= \begin{bmatrix}
\frac{1}{C_1} & 0 & 0 & 0 \\
0 & \frac{1}{C_2} & 0 & 0 \\
0 & 0 & -\frac{1}{C_3} & 0 \\
0 & 0 & 0 & -\frac{1}{C_4}
\end{bmatrix}
\begin{bmatrix}
\dot{v}_{in} \\
\dot{i}_1 \\
\dot{i}_2 \\
\dot{i}_4
\end{bmatrix}
\]

The equations (1) and (2) can be written in a simplified form as,

\[
\dot{x} = A_1x + B_1u
\]

\[
y = C_1x + D_1u
\]

2.2. Mode 2 Operation

In Mode 2, the output 2 gets charged from the input supply by turning on the switches $S_p$ and $S_2$ and the same procedure is followed to represent the differential equations in state space form shown in Equations (3) and (4).
The Equations (3) and (4) can be written in a simplified form as,

\[
\begin{align*}
\dot{x} &= A_2 x + B_2 u \\
y &= C_2 x + D_2 u \\
\end{align*}
\]

### 2.2. Mode 3 Operation

In this mode the capacitor in output 3 is getting charged by closing the switches \( S_p \) and \( S_3 \) and the associated differential equations are shown in state space form as in Equations (5) and (6).

\[
\begin{align*}
\begin{bmatrix}
\frac{1}{L} & 0 & 0 & 0 & 0 \\
-\frac{1}{C_1} & 0 & 0 & 0 & 0 \\
0 & -\frac{1}{C_2} & 0 & 0 & 0 \\
0 & 0 & -\frac{1}{C_3} & 0 & 0 \\
0 & 0 & 0 & -\frac{1}{C_4} & 0
\end{bmatrix}
\begin{bmatrix}
\dot{i}_L \\
\dot{v}_3 \\
\dot{v}_2 \\
\dot{v}_3 \\
\dot{v}_4
\end{bmatrix}
&= \begin{bmatrix}
0 & 1 & 0 & 0 & 0 \\
0 & 0 & 1 & 0 & 0 \\
0 & 0 & 0 & 1 & 0 \\
0 & 0 & 0 & 0 & 1
\end{bmatrix}
\begin{bmatrix}
i_L \\
v_1 \\
v_2 \\
v_3 \\
v_4
\end{bmatrix}
+ \begin{bmatrix}
u_1 \\
u_2 \\
u_3 \\
u_4
\end{bmatrix} + [0]u \\
\end{align*}
\]

\[
\begin{align*}
\begin{bmatrix}
\frac{1}{L} & 0 & 0 & 0 & 0 \\
0 & -\frac{1}{C_1} & 0 & 0 & 0 \\
0 & 0 & -\frac{1}{C_2} & 0 & 0 \\
0 & 0 & 0 & -\frac{1}{C_3} & 0 \\
0 & 0 & 0 & 0 & -\frac{1}{C_4}
\end{bmatrix}
\begin{bmatrix}
\dot{i}_L \\
\dot{v}_3 \\
\dot{v}_2 \\
\dot{v}_3 \\
\dot{v}_4
\end{bmatrix}
&= \begin{bmatrix}
0 & 1 & 0 & 0 & 0 \\
0 & 0 & 1 & 0 & 0 \\
0 & 0 & 0 & 1 & 0 \\
0 & 0 & 0 & 0 & 1
\end{bmatrix}
\begin{bmatrix}
i_L \\
v_1 \\
v_2 \\
v_3 \\
v_4
\end{bmatrix}
+ [0]u \\
\end{align*}
\]
The above equations (5) and (6) can be written in a simplified form as,
\[
\begin{align*}
\dot{x} &= A_3 x + B_3 u \\
y &= C_3 x + D_3 u
\end{align*}
\]

2.3. Mode 4 Operation

In Mode 4 operation, the charging of capacitor in output 4 is done by closing the switches $S_p$ and $S_4$ and the related differential equations are shown in Equations (7) and (8) in state space form.
\[
\begin{bmatrix}
\dot{i}_L \\
\dot{v}_1 \\
\dot{v}_2 \\
\dot{v}_3 \\
\dot{v}_4
\end{bmatrix} = \begin{bmatrix}
\frac{-R_{on}}{L} & 0 & 0 & 0 & -\frac{1}{L} \\
0 & -\frac{1}{R_1 C_1} & 0 & 0 & 0 \\
0 & 0 & -\frac{1}{R_2 C_2} & 0 & 0 \\
0 & 0 & 0 & -\frac{1}{R_3 C_3} & 0 \\
\frac{1}{C_4} & 0 & 0 & 0 & -\frac{1}{R_4 C_4}
\end{bmatrix}
\begin{bmatrix}
i_L \\
v_1 \\
v_2 \\
v_3 \\
v_4
\end{bmatrix} + \begin{bmatrix}
\dot{v}_{in}
\end{bmatrix}
\]

The above equations (7) and (8) can be written in simplified form as,
\[
\begin{align*}
\dot{x} &= A_4 x + B_4 u \\
y &= C_4 x + D_4 u
\end{align*}
\]

2.4. Mode 5 Operation

In Mode 5 operation the inductor current is discharged through the output 4 by closing the switches $S_p'$ and $S_4$ and the related differential equations are given in state space form in Equations (9) and (10).
\[
\begin{bmatrix}
\dot{i}_L \\
\dot{v}_1 \\
\dot{v}_2 \\
\dot{v}_3 \\
\dot{v}_4
\end{bmatrix} = \begin{bmatrix}
\frac{-R_{on}}{L} & 0 & 0 & 0 & -\frac{1}{L} \\
0 & -\frac{1}{R_1 C_1} & 0 & 0 & 0 \\
0 & 0 & -\frac{1}{R_2 C_2} & 0 & 0 \\
0 & 0 & 0 & -\frac{1}{R_3 C_3} & 0 \\
\frac{1}{C_4} & 0 & 0 & 0 & -\frac{1}{R_4 C_4}
\end{bmatrix}
\begin{bmatrix}
i_L \\
v_1 \\
v_2 \\
v_3 \\
v_4
\end{bmatrix} + \begin{bmatrix}
\dot{v}_{in}
\end{bmatrix}
\]
\[
\begin{bmatrix}
0 & 0 & 0 & 0 & 0 \\
0 & -\frac{1}{C_1} & 0 & 0 & 0 \\
0 & 0 & -\frac{1}{C_2} & 0 & 0 \\
0 & 0 & 0 & -\frac{1}{C_3} & 0 \\
0 & 0 & 0 & 0 & -\frac{1}{C_4}
\end{bmatrix}
\begin{bmatrix}
v_1 \\
v_2 \\
v_3 \\
v_4 \\
v_{in}
\end{bmatrix} = \begin{bmatrix}
\frac{1}{L}i_1 \\
\frac{1}{L}i_2 \\
\frac{1}{L}i_3 \\
\frac{1}{L}i_4 \\
0
\end{bmatrix} + [0]u
\] (9)

\[
\begin{bmatrix}
v_1 \\
v_2 \\
v_3 \\
v_4
\end{bmatrix} = \begin{bmatrix}
0 & 1 & 0 & 0 \\
0 & 0 & 1 & 0 \\
0 & 0 & 0 & 1 \\
0 & 0 & 0 & 0
\end{bmatrix} \begin{bmatrix}
i_1 \\
i_2 \\
i_3 \\
i_4
\end{bmatrix} + [0]u
\] (10)

The above equations (9) and (10) are written in a simplified form as,

\[
\begin{align*}
\dot{x} &= Ax + Bu \\
y &= Cx
\end{align*}
\] (11)

As the converter switches among the five modes for each switching cycle, the averaged representation of the system is written through equation (11)

where

\[
A = A_1D_1 + A_2D_2 + A_3D_3 + A_4D_4 + A_5(1 - D_1 - D_2 - D_3 - D_4)
\]

\[
B = B_1D_1 + B_2D_2 + B_3D_3 + B_4D_4 + B_5(1 - D_1 - D_2 - D_3 - D_4)
\]

\[
C = C_1D_1 + C_2D_2 + C_3D_3 + C_4D_4 + C_5(1 - D_1 - D_2 - D_3 - D_4)
\]
3. SMALL SIGNAL PERTURBATION AND LINEARIZATION

To analyze the stability of a non-linear circuit for normal operating condition with small deviations, linear models are developed by approximately linearizing the circuit. The linear model which also can be called as small signal ac model is developed for non-ideal SIQO dc-dc buck converter at the quiescent operating point \((I, V)\) assuming that \(U\) and the duty ratios are equal to the chosen quiescent values together with superimposed small ac variations. The Table 1 gives the list of system variables considered to develop small signal ac model.

\[
\begin{align*}
C &= \begin{bmatrix}
0 & 1 & 0 & 0 & 0 \\
0 & 0 & 1 & 0 & 0 \\
0 & 0 & 0 & 1 & 0 \\
0 & 0 & 0 & 0 & 1
\end{bmatrix}
\end{align*}
\]

<table>
<thead>
<tr>
<th>Input voltage</th>
<th>Output voltages</th>
<th>Load currents</th>
<th>Duty ratios</th>
</tr>
</thead>
<tbody>
<tr>
<td>(v_{in}) = (V_{in} + v_{in})</td>
<td>(v_1 = V_i + \bar{v}_1)</td>
<td>(i_1 = i_1 + \bar{i}_1)</td>
<td>(d_1 = d_1 + \bar{d}_1)</td>
</tr>
<tr>
<td>(v_2 = v_2 + \bar{v}_2)</td>
<td>(i_2 = i_2 + \bar{i}_2)</td>
<td>(d_2 = d_2 + \bar{d}_2)</td>
<td></td>
</tr>
<tr>
<td>(v_3 = v_3 + \bar{v}_3)</td>
<td>(i_3 = i_3 + \bar{i}_3)</td>
<td>(d_3 = d_3 + \bar{d}_3)</td>
<td></td>
</tr>
<tr>
<td>(v_4 = v_4 + \bar{v}_4)</td>
<td>(i_4 = i_4 + \bar{i}_4)</td>
<td>(d_4 = d_4 + \bar{d}_4)</td>
<td></td>
</tr>
</tbody>
</table>

It is known that the small signal analysis follows the equation (11) and appropriate substitutions lead to Equations (12) and (13) and yield the final lumped equivalent small signal circuit of the SIQO converter in Figure 9.

\[
x = x + \dot{x} \quad (12)
\]

\[
\dot{x} + A\dot{x} = A_1(D_1 + \bar{d}_1) + A_2(D_2 + \bar{d}_2) + A_3(D_3 + \bar{d}_3) + A_4(D_4 + \bar{d}_4) + A_5(1 - D_1 - D_2 - D_3 - D_4 - \bar{d}_1 - \bar{d}_2 - \bar{d}_3 - \bar{d}_4)(x + \bar{x}) + B_1\dot{D}_1 + B_2\dot{D}_2 + B_3\dot{D}_3 + B_4\dot{D}_4 + B_5(1 - D_1 - D_2 - D_3 - D_4 - \bar{d}_1 - \bar{d}_2 - \bar{d}_3 - \bar{d}_4)(u + \bar{u}) \quad (13)
\]

\[
\dot{x} = A\dot{x} + [BE_1E_2E_3E_4]d_1, \quad \dot{d}_2, \quad \dot{d}_3, \quad \dot{d}_4
\quad (14)
\]

where

\[
E_1 = \begin{bmatrix}
\frac{L}{I_c} & \frac{L}{I_c} & 0 \\
\frac{L}{I_c} & \frac{L}{I_c} & 0 \\
-\frac{I_c}{C_1} & -\frac{I_c}{C_2} & 0
\end{bmatrix} \quad E_2 = \begin{bmatrix}
\frac{L}{I_c} & \frac{L}{I_c} & 0 \\
\frac{L}{I_c} & \frac{L}{I_c} & 0 \\
-\frac{I_c}{C_2} & -\frac{I_c}{C_3} & 0
\end{bmatrix} \quad E_3 = \begin{bmatrix}
\frac{L}{I_c} & \frac{L}{I_c} & 0 \\
\frac{L}{I_c} & \frac{L}{I_c} & 0 \\
-\frac{I_c}{C_3} & -\frac{I_c}{C_4} & 0
\end{bmatrix} \quad E_4 = \begin{bmatrix}
\frac{L}{I_c} & \frac{L}{I_c} & 0 \\
\frac{L}{I_c} & \frac{L}{I_c} & 0 \\
-\frac{I_c}{C_4} & -\frac{I_c}{C_4} & 0
\end{bmatrix}
\]

The developed small signal equivalent circuit helps to obtain the control to output transfer functions. To obtain the transfer function of output1 to \(d_1\), the reduced equivalent circuit is drawn by making the other duty ratios and the other load currents as zero. The numerical values of the parameters of the SIQO compensator based performance enhancement strategy for a SIQO buck converter (S. Augusti Lindiya)
The converter in Table 2 are used to obtain the transfer function model shown in Equations (15) to (18), one for each output by using MATLAB® M-file coding with the help of small signal state space model.

![Diagram of the converter](image)

Figure 9. Lumped equivalent small-signal circuit of the converter

<p>| Table 2. The parameters of the SIQO Buck converter |</p>
<table>
<thead>
<tr>
<th>Parameters</th>
<th>Symbol</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Voltage</td>
<td>$V_{in}$</td>
<td>12 V</td>
</tr>
<tr>
<td>Switching Frequency</td>
<td>$f_s$</td>
<td>33 kHz</td>
</tr>
<tr>
<td>Inductance</td>
<td>$L$</td>
<td>51 μH</td>
</tr>
<tr>
<td>Capacitance 1</td>
<td>$C_1$</td>
<td>2200 μF</td>
</tr>
<tr>
<td>Capacitance 2</td>
<td>$C_2$</td>
<td>1000 μF</td>
</tr>
<tr>
<td>Capacitance 3</td>
<td>$C_3$</td>
<td>1000 μF</td>
</tr>
<tr>
<td>Capacitance 4</td>
<td>$C_4$</td>
<td>3300 μF</td>
</tr>
<tr>
<td>Output Voltage 1</td>
<td>$V_1$</td>
<td>1 V</td>
</tr>
<tr>
<td>Output Voltage 2</td>
<td>$V_2$</td>
<td>1.2 V</td>
</tr>
<tr>
<td>Output Voltage 3</td>
<td>$V_3$</td>
<td>1.8 V</td>
</tr>
<tr>
<td>Output Voltage 4</td>
<td>$V_4$</td>
<td>3.3 V</td>
</tr>
</tbody>
</table>

\[ G_1(s) = \frac{\Delta_1(s)}{\Delta_2(s)} = \frac{2273.5^4+1.841\times10^7s^3+3.591\times10^{10}s^2+2.518\times10^{13}s+5.517\times10^{16}}{s^5+5976.5^4+1.397\times10^{15}s^2+1.423\times10^{17}s+6.237\times10^{12}s+9.708\times10^{14}} \] (15)

\[ G_2(s) = \frac{\Delta_2(s)}{\Delta_3(s)} = \frac{5000.5^4+3.443\times10^{15}s^3+6.960\times10^{17}s^2+5.249\times10^{20}s+1.247\times10^{23}}{s^5+5976.5^4+1.397\times10^{15}s^2+1.423\times10^{17}s+6.237\times10^{12}s+9.708\times10^{14}} \] (16)

\[ G_3(s) = \frac{\Delta_3(s)}{\Delta_4(s)} = \frac{5000.5^4+4.39\times10^{15}s^3+6.639\times10^{17}s^2+3.443\times10^{20}s+5.847\times10^{23}}{s^5+5976.5^4+1.397\times10^{15}s^2+1.423\times10^{17}s+6.237\times10^{12}s+9.708\times10^{14}} \] (17)

\[ G_4(s) = \frac{\Delta_4(s)}{\Delta_5(s)} = \frac{6.118\times10^{15}s^3+1.145\times10^{23}s^2+6.488\times10^{25}s+1.159\times10^{28}}{s^5+5976.5^4+1.397\times10^{15}s^2+1.423\times10^{17}s+6.237\times10^{12}s+9.708\times10^{14}} \] (18)
To test the accuracy of the developed mathematical model of the converter the output voltage \( V_4 \) and Inductor Current (Average value) \( I_L \) are observed by varying \( D_0 \) and \( D_4 \) while keeping \( D_1 = 0.32 \), \( D_2 = 0.024 \) and \( D_3 = 0.072 \). The observations as variations in output voltage and inductor current due to change in duty ratios are shown in Table 3.

It is inferred from Table 3 that a linear increase is observed in \( I_L \) and \( V_4 \) due to increase in the duration of inductor current charging. Similarly the output voltages one and four are observed by varying \( D_1 \) and \( D_4 \) keeping \( D_0 = 0.32 \), \( D_2 = 0.024 \) and \( D_3 = 0.072 \) and the readings are tabulated in Table 4.

| Table 3. Variation in output voltage and inductor current due to change in duty ratios |
|----------------------------------|-----|-----|-----|-----|-----|
| \( D_0 \) = 0.28 | \( D_0 \) = 0.30 | \( D_0 \) = 0.32 | \( D_0 \) = 0.34 | \( D_0 \) = 0.36 |
| \( D_1 \) = 0.138 | \( D_1 \) = 0.158 | \( D_1 \) = 0.178 | \( D_1 \) = 0.198 | \( D_1 \) = 0.218 |
| \( V_4 \) | \( I_L \) | \( V_4 \) | \( I_L \) | \( V_4 \) | \( I_L \) | \( V_4 \) | \( I_L \) | \( V_4 \) | \( I_L \) |
| Model | 4.4 | 3 | 4.6 | 3.3 | 4.8 | 3.3 | 4.8 | 3.5 | 5 | 3.8 |
| Simulation | 4.0 | 2.9 | 4.2 | 3.1 | 4.6 | 3.1 | 4.6 | 3.3 | 4.8 | 3.5 |

| Table 4. Variation in output voltages due to change in duty ratios: |
|----------------------------------|-----|-----|-----|-----|-----|
| \( D_1 \) = 0.042 | \( D_1 \) = 0.044 | \( D_1 \) = 0.046 | \( D_1 \) = 0.048 | \( D_1 \) = 0.05 |
| \( D_4 \) = 0.182 | \( D_4 \) = 0.180 | \( D_4 \) = 0.178 | \( D_4 \) = 0.176 | \( D_4 \) = 0.174 |
| \( V_1 \) | \( V_4 \) | \( V_1 \) | \( V_4 \) | \( V_1 \) | \( V_4 \) | \( V_1 \) | \( V_4 \) | \( V_1 \) | \( V_4 \) |
| Model | 0.8 | 3.5 | 0.8 | 3.5 | 0.8 | 3.52 | 0.76 | 3.52 | 0.75 | 3.53 |
| Simulation | 0.9 | 3.3 | 1.01 | 3.3 | 1.0 | 3.3 | 1.0 | 3.3 | 1.0 | 3.3 |

It is inferred from Table 4 that the output voltages are almost remain same as the charging period of the inductor current maintained constant. This proves that the system represented by mathematical model developed and discrete components are same with small deviations observed due to non-ideal components. Therefore a model is developed in this research for four outputs and verified.

4. COMPENSATOR DESIGN

The design of compensator revolves around two significant issues that include an enhancement in the stability of the converter system and therefrom derive an acceptable time response. In order to obtain the desired phase margin and to increase the steady state accuracy of the system, a compensator \( G_c(s) \) is added in between the error detector and the systems \( G(s) \). The block diagram representation of the closed loop system is shown in Figure 10 [16].

![Figure 10. Block diagram representation of closed loop system](image)

In Figure 10 \( R(s) \) is the reference input and \( C(s) \) is the system output. The design of compensator attempts to remove the steady state error without disturbing the stability properties. The main contribution from the user end reiterates the need to focus on the choice of compensators for extricating an enhancement in both time and frequency domain responses. The codes written in the MATLAB® portal enable to obtain the Bode plots and the step response for the Equations (15), (16), (17) and (18) which help to obtain the classical stability criteria’s such as phase and delay margins and gain crossover frequency and time response specifications. Compensators are designed with the help of MATLAB® SISO tool GUI to obtain the reasonable values of the performance specifications. Lag compensators are added to all the outputs such that
steady state error is removed [16]. The low frequency gain of the system is changed until the desired phase margin which should be in between 45 degree to 60 degree is obtained. The zero of the compensator is placed such that the zero dB gain cross over frequency should be in between 1/5 to 1/8 of switching frequency. The Equations (19), (20), (21) and (22) are the lag compensators obtained for four outputs respectively. The time and frequency domain specifications of the system with lag compensators are given in Table 5. It is inferred from Table 5 that the outputs have peak overshoot which is in the order of 20%.

\[
G_{c1} = 20 \frac{s+7320}{s+732} \qquad (19)
\]

\[
G_{c2} = 5.5 \frac{s+6320}{s+632} \qquad (20)
\]

\[
G_{c3} = 8 \frac{s+8240}{s+824} \qquad (21)
\]

\[
G_{c4} = 0.5 \frac{s+2000}{s+200} \qquad (22)
\]

In order to reduce the peak overshoot, lag-lead compensators are designed as given in Equations (23), (24), (25) and (26) for all the outputs and the performance specifications are tabulated in Table 5. As lead compensator is also added along with lag compensator to reduce the peak overshoot, there will be increase in phase margin as lead compensator contributes phase into the system.

\[
G_{c1}(s) = 4.5 \frac{(s+7320)}{(s+732)} \qquad (23)
\]

\[
G_{c2} = 11 \frac{s+7071}{s+1.414e04} \frac{s+6320}{s+632} \qquad (24)
\]

\[
G_{c3} = 16 \frac{s+7071}{s+1.414e04} \frac{s+8240}{s+824} \qquad (25)
\]

\[
G_{c4} = 11 \frac{s+7320}{s+732} \frac{s+7071}{s+1.414e04} \qquad (26)
\]

Figure 11 and Figure 12a, b, c and d show the Bode plots and step responses of the dc-dc converter for four outputs with and without lag-lead compensator respectively. From the Bode plots shown in Figure 11, it is clear that the addition of lead compensator along with lag compensator will increase the phase margin but the desired peak overshoot and gain crossover frequency are obtained.

The step response of the fur outputs with and without compensator is shown in Figure 12 plots reveal that the reduced peak overshoot, less rise time and settling time and zero steady state error are obtained due to the addition of lag lead compensators. Introduction of lag compensator bring the system phase margin to an acceptable value of around 55 degree and desired time response characteristics except percentage peak overshoot. However, the addition of lag-lead compensator will further improve the time response parameters, gain crossover frequency, delay margin and also reduce the peak overshoot but contribute a considerable change in phase margin. The power circuit developed in MATLAB/Simulink using discrete components with the designed compensator and the observed output voltages is shown in Figure 13.

Figure 13. Simulated output Voltages response of the SIQO converter
Compensator Based Performance Enhancement Strategy for a SIQO Buck Converter (S. Augusti Lindiya)

Figure 11. Magnitude and Phase response of the outputs with and without compensator
(a) $V_1$ (b) $V_2$ (c) $V_3$ (d) $V_4$

The closeness of the four output voltages response obtained through the use of discrete components from simulation in Figure 13 with that in Figure 12 serves to validate the modeling of the converter and design of the compensator.

Figure 12. Step response of the outputs with and without compensator (a) $V_1$ (b) $V_2$ (c) $V_3$ (d) $V_4$
5. HARDWARE IMPLEMENTATION

In the Section 4, the dc-dc converter and the compensators which are incorporated in four outputs are discussed and their performance study is done using MATLAB® M-file coding. However it is necessary to verify these results by hardware implementation and it is explained in this section. The output voltages of the converter are given to the analog input of the data acquisition module DT9834® which is interfaced to MATLAB/Simulink®. Then the output voltages are compared with the reference voltages and the error signal is applied to the compensator developed in MATLAB/Simulink® and the control voltage signals are applied to the analog output of the DAQ module. The pulse width modulation generator and driver circuit avails the data from DAQ module to generate the pulses for the IGBT switches in the power module. The experimental hardware setup of SIQO converter seen through the photograph in Figure 14 is constructed and tested for the same specifications as those used in simulation.

![Figure 14. Hardware test setup of SIQO converter with compensator](image)

Figure 14. Hardware test setup of SIQO converter with compensator

Figure 15 represents the PWM pulses for the main path obtained from PWM generator and driver circuit using the reference signal obtained from Data Acquisition Module.

![Figure 15. PWM pulses for main path](image)

Figure 15. PWM pulses for main path

Figure 16 shows the output voltages obtained from the model which can be observed in the scope connected to the analog input of Data Acquisition Module. Table 6 compares the performance of the SIQO converter as a function of the output voltage, voltage regulation and ripple in the output voltages acquired.
through simulation and from the hardware module to ensure the viability of the system to operate over a range of loads.

![Image of output voltages](image)

Figure 16. Output voltages of the SIQO converter from Prototype Model

<table>
<thead>
<tr>
<th>Table 6. Performance of SIQO converter obtained by simulation and hardware</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sl.No.</td>
</tr>
<tr>
<td>1</td>
</tr>
<tr>
<td>0.6</td>
</tr>
<tr>
<td>1.8</td>
</tr>
<tr>
<td>6.6</td>
</tr>
<tr>
<td>2</td>
</tr>
<tr>
<td>0.55</td>
</tr>
<tr>
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<tr>
<td>0.65</td>
</tr>
<tr>
<td>2.025</td>
</tr>
<tr>
<td>7.26</td>
</tr>
</tbody>
</table>

It is inferred that the compensator is able to maintain the output voltages constant against the load disturbances and the ripples are maintained at small value. Moreover the output voltages will not be disturbed by the disturbances present at other outputs.

6. CONCLUSION

A single input four output dc-dc buck converter with single inductor is designed which results in low cost and less space. SIMO converters in the open loop operation result in poor performance under steady state and transient conditions. To improve the performance a compensator is to be added to the converter. To design compensators the four output dc-dc buck converter has been modeled in the state space framework and its small signal equivalent circuit is derived over a chosen quiescent point. The transfer function model has also been obtained to realize the Bode plot for the system and therefrom enable the choice of compensators.

The simulation study has been presented to demonstrate the function of the compensators and benign its benefits through improvements in time response specifications. As the designed lag-lead compensators are not able to satisfy both phase margin and peak overshoot, it is recommended to design multivariable controller using optimization technique which is the extension of this work. With the compensators incorporated in each output steady state output voltages are observed using...
MATLAB/Simulink®. The prototype using DT9834® DAQ module results have been garnered to correlate the simulated performance and evince a place for the use of the converter in the practical world.

REFERENCES

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