An Ultra Low Power CMOS Sigma Delta ADC Modulator for System-on-chip (SoC) Temperature Sensor for Aerospace Applications

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ABSTRACT
In the current paper, an accurate with low power consumed sigma delta (ΣΔ) analog to digital converter has been designed for the aerospace applications. The sigma delta ADC has been designed in such a way that it works fine with consumption of low power and high accuracy in the system on chip (SoC) temperature sensor where the analog output from the temperature sensor unit will be the fed to the analog to digital converter. To check the robustness, different parameters with variation has been analyzed. The high gain operational amplifier plays a vital role in the circuit design. Hence, a 30 MHz operational amplifier has also been proposed whose unity gain bandwidth (UGB) has been observed of about 30 MHz, 51.1 dB dc gain and slew rate (SR) of about 27.9 V/µsec. For the proper operation of the circuit, a power supply of +1.3V to -1.3V is used. The proposed sigma delta ADC modulator is showing better results over previously designed modulator in terms of power consumption, error and performance. The design and simulation have been tested with the help of cadence analog design environment with UMC 90nm CMOS process technology.

Keywords: Clocked comparator, CMOS, DAC, Integrator, Op-amp, Signal to Noise Ratio (SNR)

1. INTRODUCTION
The continuous innovation of technology has demanded an entire circuit system to be embedded on a single chip. System-on-chip temperature sensor requires a high performance, least inaccurate, more efficient, reliable and robust analog to digital converter which can be used to convert the analog signal receiving from the temperature sensor into digital domain. The data in digital domain is much safer, can be transferred, copied easily compared to analog domain. In terms of accuracy and high signal to noise ratio (SNR), sigma delta (ΣΔ) ADC is the best choice in compared to available ADC as they cannot gain very high accuracy. The sigma delta (ΣΔ) ADC comprises of two part i.e. sigma delta modulator and digital filter. The modulator part combines sampling at the rate equal and above to Nyquist rate and the preceding digital filter exchanges the amplitude for the resolution in time. Furthermore, sigma delta (ΣΔ) ADC has a capability to tolerate the imperfection of analog circuit up to great extend. Sigma delta (ΣΔ) provides the implementation of high density and complex analog circuit.

Therefore it becomes the first priority to realize in system-on-chip (SoC). The block diagram of sigma delta modulator is shown in Figure 1. The designed sigma delta (ΣΔ) ADC modulator consists of an integrator. The forward path of high order sigma delta (ΣΔ) ADC modulator contains more than one integrator which no doubt offers great resolution but unfortunately it suffers from potential instability [1], [2]. However, single order sigma delta (ΣΔ) ADC modulator may be cascaded to get precise gain. The order of sigma delta (ΣΔ) ADC modulator varies with its applications. The input signal to sigma delta (ΣΔ) ADC
modulator is sampled at high frequency and thus the conversion of analog signal into digital pulse takes place. The bad filtering process result into generation of digital pulse engulfed of unwanted noise [3], [4].

![Block diagram of sigma delta modulator](image)

The resolution of obtained output is directly dependent on the order of modulator and the sampling ratio which is decided at the modulator stage. Earlier the anti-aliasing filter was being considered but the principle of oversampling ratio ends the requirement of it, since now the analog input signal can be sampled directly using oversampling clock [6], [7]. Hence, an improved and accurate ultra low power sigma delta (ΣΔ) ADC modulator has been designed and argued in this paper. The rest of the article is patterned as follows. Section II enlightens the proposed circuit’s configuration with the detailed depiction of each unit. Section III is dedicated to the results and discussion. Finally, section IV wraps up the work and the article ends with conclusions and acknowledges to the funding agency Indian Space Research Organization (ISRO) (India). The sigma delta (ΣΔ) ADC modulator shown in Figure 1 consists of a difference amplifier, an integrator, a comparator, a D flip flop and a DAC in the feedback loop of the modulator. The input analog signal has been passed through several processes like oversampling, quantization and noise shaping before it comes into pulse train at output. Both the conversion processes i.e. analog to digital (ADC) and digital to analog (DAC) conserves a vital space in modern technology [8], [9].

2. **PROPOSED CIRCUIT CONFIGURATION**

2.1. **Operational Amplifier**

The wide applications of operational amplifier make it a key ingredient to many analog systems. Basically it consists of a differential amplifier which amplifies the difference between two input signals. The differential amplifier also provides a required gain. To further improvise the gain of an operational amplifier, a second stage of common source stage is attached. Miller compensation technique has been implemented here for the stability of system. On the other hand, coupling capacitor found it place inbetween the common source amplifier’s input and final stage of differential amplifier. Figure 2 shows the schematic of proposed operational amplifier. Mostly the feedback in operational amplifier is imposed to make the transfer function of system independent of gain. But in high frequency applications, as the frequency increases, gain slightly decreases and making transfer function unstable. To avoid this unstability, op-amps must be chosen of broad band for high frequency applications. The sizes of different transistors used in Figure 2 are tabulated in Table 1.

The two stage architecture has the disadvantage of having two impedance nodes which are indicated by A and B due to which two pole will be dominant which will deteriorate the phase margin of the op amp. Hence, a Miller capacitance (C_c) has been introduced between A and B to resolve it. The chosen value must satisfy the following equation [10].

\[
C_c = \frac{2.2}{10} C_L
\]

Where, coupling capacitor is denoted by C_c while load capacitorn is expressed as C_L. Similarly, the unity gain bandwidth product (GB) is termed as,

\[
B = \frac{\theta m^2}{C_c}
\]
Where, $g_{m1}$ is the input transconductance. For the gain-bandwidth product to be high the input transconductance should be high, by making the channels of MN1 and MN2 wide. Similarly the output capacitance should be low.

![Proposed schematic of Op-amp](image)

Figure 2. Proposed schematic of Op-amp

Variation in W and L can be made by using following Equation (3).

$$g_m = \sqrt{2\mu_p C_{ox} \frac{W}{L} I_d}$$

SLew Rate decides the current flowing in the transistor MN5, and is determined by how fast can be charged and discharged. This is given by Equation (4)

$$\text{Slew Rate} = \frac{I_s}{C_C}$$

The aspect ratio of transistor MP3 is decided by the positive input common mode range. Output pole should be assumed at the location which is approx 2.2 times for phase margin of 60°. Hence, $g_{m6}$ is determined by the following Equation (5)

$$g_{m6} = 2.2g_{m2} \left(\frac{C_I}{C_C}\right)$$

<table>
<thead>
<tr>
<th>Table 1 Sizes of Transistor Utilized in Circuit 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transistor</td>
</tr>
<tr>
<td>------------</td>
</tr>
<tr>
<td>MP1</td>
</tr>
<tr>
<td>MP2</td>
</tr>
<tr>
<td>MP3</td>
</tr>
<tr>
<td>MP4</td>
</tr>
<tr>
<td>MN1</td>
</tr>
<tr>
<td>MN2</td>
</tr>
<tr>
<td>MN3</td>
</tr>
<tr>
<td>MN4</td>
</tr>
<tr>
<td>MN5</td>
</tr>
<tr>
<td>MN6</td>
</tr>
</tbody>
</table>
2.2. Difference amplifier and integrator

Difference amplifier comes under the list of applications of operational amplifier. The design of difference amplifier uses two stage operational amplifier. Since it shows good voltage gain, CMRR, slew rate, it is adopted here. The difference amplifier is basically having two input terminals i.e. $V_2$ and $V_1$ and one output terminal ($V_{out}$). The output is the difference of the two inputs. On the other hand, The CMOS integrator performs mathematical operation on input and produces an output which is proportion to the integral of the input voltage. Figure 3 and 4 show the schematic of difference amplifier and integrator. Integrator is the important building block used in the design of continuous time filters [11]. The change in the combination of resistance and capacitor values changes the value of RC time constant which further affects the rate of change of output voltage.

![Figure 3 Schematic of difference amplifier](image1)

![Figure 4 Schematic of integrator](image2)

Ideally the summation of previous output $v(kT - T)$ and previous input $u(kT - T)$ gives the the output of the integrator

$$v(kT) = g_0 u(kT - T) + v(kT - T)$$

The constant $g_0$ represents the gain preceding the input to integrator. Equation (6) is corresponding to the transfer function of an ideal integrator shown in Equation (7).

$$H(z) = \frac{g_0 z^{-1}}{1 - z^{-1}}$$

2.3. Comparator

In compare to other units of sigma delta ($\Sigma\Delta$) ADC modulator, comparator is the most fundamental component as the comparison of two different analog inputs signal and make out of single digital output signal have been done in this unit. It has a vital impact on the performance and reliability of the designed circuit. The schematic of proposed comparator is shown in Figure 5. The input offset voltage, delay and the range of the input signal decides the speed and resolution of analog to digital converter [12].The basic property of the comparator is to take the analog input and gives a binary or digital output. Clocked comparators are often called dynamic comparator. Regenerative feedback is often used in dynamic comparator and occasionally in non clocked comparator. Dynamic comparator is used in the design of high speed ADCs.

2.4. D flip flop

The used D flip flop has three interconnected RS latch circuits. In designing, any of NAND or NOR can be used. When clock gets logic 1, the output latch gets isolated from any input changes as the output of the two middle input gates is forced to get logic 0. On the other hand, the input latch with an illegal state will automatic resume its latching action, when logic 0 is triggered by clock. Figure 6 depicts the schematic of proposed D flip-flop.

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2.5. 1 bit DAC

Basically digital signal or code is converted into analog voltage or current by using digital to analog converter (DAC). The DAC is comprised of reference voltage ($V_{ref}$), supply voltage ($V_{dd}$) and analog output. True analog quantity has not been observed at the output of the digital to analog converter (DAC).
The schematic of proposed 1 bit DAC is shown in Figure 7. The output is found in pseudo analog quantity. The number of input bits should be increased, since the obtained analog output is proportional to its digital pulse input. Therefore the step size gets reduced and due to higher number of bits, the output seems to be analog signal.

![Proposed schematic of 1 bit DAC](image)

**Figure 7** Proposed schematic of 1 bit DAC

3. **RESULTS AND ANALYSIS**

The components and the final designed sigma delta modulator are simulated using UMC 90nm. The output gain of operational amplifier is depicted in Figure 8. While the simulated results of difference amplifier (Figure 9), integrator (Figure 10), Comparator (Figure 11), D flip-flop (Figure 12), 1 bit DAC (Figure 13) and sigma delta modulator (Figure 14) are shown below.

![Output gain of operational amplifier](image)

**Figure 8.** Output gain of operational amplifier

![Output result of difference amplifier](image)

**Figure 9.** Output result of difference amplifier
Figure 10 Output result of integrator

Figure 11 Output result of clocked comparator

Figure 12 Output result of D flip flop

Figure 13 Output result of 1 bit DAC
Table 2 Comparison with Some Other Recent Work

<table>
<thead>
<tr>
<th>Factor</th>
<th>[5]</th>
<th>[13]</th>
<th>[14]</th>
<th>[16]</th>
<th>[17]</th>
<th>[18]</th>
<th>[15]</th>
<th>[19]</th>
<th>This Work</th>
</tr>
</thead>
<tbody>
<tr>
<td>Process Technology</td>
<td>0.18µm CMOS</td>
<td>130nm CMOS</td>
<td>180nm CMOS</td>
<td>MATLAB</td>
<td>0.18µm CMOS</td>
<td>0.35nm CMOS</td>
<td>0.35 µm CMOS</td>
<td>0.13nm CMOS</td>
<td>90nm CMOS</td>
</tr>
<tr>
<td>Architecture</td>
<td>Flash</td>
<td>Sigma</td>
<td>Delta</td>
<td>Sigma</td>
<td>Sigma</td>
<td>Delta</td>
<td>Delta</td>
<td>Flash</td>
<td>Flash</td>
</tr>
<tr>
<td>Input Voltage</td>
<td>0 to 1.8V</td>
<td>1V</td>
<td>2V</td>
<td>1V</td>
<td>3.3V</td>
<td>3V</td>
<td>1.5V</td>
<td>1.3V</td>
<td></td>
</tr>
<tr>
<td>SNR</td>
<td>---</td>
<td>78dB</td>
<td>---</td>
<td>82dB</td>
<td>85.2dB</td>
<td>85dB</td>
<td>73 dB</td>
<td>--</td>
<td>62dB</td>
</tr>
<tr>
<td>Power dissipated</td>
<td>36.23mW</td>
<td>68µW</td>
<td>6.45µW</td>
<td>--</td>
<td>1.96mW</td>
<td>200mA</td>
<td>341mW</td>
<td>160mA</td>
<td>54µW</td>
</tr>
</tbody>
</table>

4. CONCLUSION

In the present paper, an ultra low power sigma delta (ΣΔ) ADC modulator which is highly useful in system on chip (SOC) temperature sensor for aerospace applications has been described. Comparison of work done in this paper has been compared in Table 2. The each unit of sigma delta delta (ΣΔ) ADC modulator is examined and modeled here. The proposed sigma delta delta (ΣΔ) ADC modulator works utilizing minimal power supply of +1.3V to -1.3V. The average power of 54 µW is dissipated with the sampling frequency of 50MHz.

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REFERENCES


**BIBLIOGRAPHY OF AUTHORS**

Deepak Prasad was born in Dhanbad (Jharkhand) India in 1990. He received his Bachelor degree in Electronics and Communication Engineering from RGPV Bhopal in 2012 and Master degree in Electronics and Instrumentation from The Burdwan University in 2015. He has completed his M Tech project work from CSIR-Central Institute of Mining & Fuel Research (CIMFR), Dhanbad on the topic of “Design strata deformation indicator for underground coal mines” under the guidance of Senior Scientist Dr. P. K. Mishra. He has qualified GATE 2013 and GATE 2015 successfully. Presently he is working as Junior Research Fellow in ISRO Project entitled “Design of ultra low power CMOS (Complementary Metal Oxide Semiconductor) temperature sensor for aerospace application”. He is also pursuing PhD on the same topic under the guidance of Dr. Vijay Nath, Department of Electronics and Communication Engineering, Birla Institute of Technology, Mesra Ranchi, Jharkhand. His research area includes analog, digital, mixed CMOS VLSI circuits, low power VLSI circuits, ADC, DAC, PTAT circuits. His design is selected in Top 6 all India Cadence Design Contest-2016 organized by Cadence Company Ireland. He has around 8 publications in national and international conferences.

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